IN THE CLAIMS

Please amend claims 1-4, 6-7, 10, 12-13, 17-19, 27, 33, and 37 as follows below.

Please cancel claim 11 without prejudice.

Please add new claims 42-60 as follow below.

The following listing of claims replaces all prior versions, and listings, of claims in the application:

MARKED UP VERSION OF CLAIMS

1. (Currently Amended) A method comprising:

receiving a plurality of localized measures of activity in an integrated circuit;

generating a measure of global functional activity in [[an]] the integrated circuit responsive to the plurality of localized measures of activity;

determining if a predetermined limit of ~~global functional~~ activity ~~in the integrated circuit~~ has been met or exceeded by the measure of global functional activity in the integrated circuit;

and if so, then

gradually reducing a high frequency of clocking of circuitry to zero to stop the clocking of circuitry,

waiting a first predetermined time after stopping the clocking of circuitry, and

starting the clocking of circuitry at a low frequency.

2. (Currently Amended) The method of claim 1, wherein

if ~~the determining if~~ the predetermined limit of ~~global functional~~ activity ~~in the integrated circuit~~ has not been met or exceeded by the measure of global functional activity, ~~it is repeated~~ repeating the receiving, the generating, and the determining.

3. (Currently Amended) The method of claim 1, wherein

the first predetermined time is a number of clock cycles of a free-running clock of the integrated circuit.

4. (Currently Amended) The method of claim 1 wherein,

the gradual reducing of the high frequency clocking of circuitry to zero includes

clocking circuitry at a first frequency, and,

before clocking the circuitry at a second frequency lower than the first frequency,

waiting a second predetermined time during the clocking of the circuitry at the first frequency.

5. (Original) The method of claim 1, wherein,
after starting the clocking of the circuitry at the low frequency, the method further includes
gradually increasing the frequency of the clocking of the circuitry to the high frequency.

6. (Currently Amended) The method of claim 5 wherein,
the gradual increasing of the frequency of the clocking of circuitry to the high frequency includes
clocking circuitry at a first frequency, and,
before clocking the circuitry at a second frequency higher than the first frequency,
waiting a second predetermined time during the clocking of the circuitry at the first frequency.

7. (Currently Amended) The method of claim 1, wherein,
an estimated temperature level of the integrated circuit is proportional to the global functional activity in the integrated circuit and
the predetermined limit of ~~global functional~~ activity is proportional to an expected temperature level of the integrated circuit.

8. (Previously Presented) The method of claim 1, wherein

the gradual reducing of the high frequency clocking of the circuitry to zero avoids large variations in current otherwise associated with a rapid shut-off of the clocking of circuitry.

9. (Original) The method of claim 5, wherein

the starting of the clocking of the circuitry at the low frequency and the gradual increase in the frequency of the clocking of the circuitry to the high frequency avoids large variations in current otherwise associated with a rapid turn-on of the clocking of circuitry.

10. (Currently Amended) An integrated circuit comprising:

a clock generator to generate a clock;

an activity detector to receive a plurality of localized measures of activity of functional blocks in the integrated circuit and generate a measure of global functional activity of the integrated circuit responsive to the plurality of localized measures of activity; and

a clock throttling controller coupled to the activity detector and the clock generator, the clock throttling controller to generate a throttled clock to couple to the

functional blocks of the integrated circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to the functional blocks in response to the measure of the global functional activity meeting or exceeding a predetermined limit of activity.

11. (Canceled)

12. (Currently Amended) The integrated circuit of claim 10, wherein,

~~the activity detector receives measures of local functional activity associated with each functional block of the integrated circuit to determine the measure of the global functional activity of the integrated circuit,~~

the activity detector compares the measure of the global functional activity with the predetermined limit of activity to determine if it is met or exceeded, and

the activity detector signals to the clock throttling controller whether or not the predetermined limit of activity has been met or exceeded.

13. (Currently Amended) An [[The]] integrated circuit ~~of claim 10, further~~ comprising: [[,]]

a clock generator to generate a clock;

an activity detector to measure global functional

activity of the integrated circuit;

a clock throttling controller coupled to the activity detector and the clock generator, the clock throttling controller to generate a throttled clock to couple to functional blocks of the integrated circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to the functional blocks in response to the measure of the global functional activity meeting or exceeding a predetermined limit; and

a logical gate coupled to the clock generator and the clock throttling controller, the logical gate to receive the clock from the clock generator and a control signal from the clock throttling controller, the logical gate to periodically mask out one or more clock cycles of the clock to generate the throttled clock in response to the control signal [[, to]] and gradually throttle down the frequency of the throttled clock.

14. (Previously Presented) The integrated circuit of claim 13, wherein,

the logical gate is an AND gate to logically AND the clock and the control signal from the clock throttling controller together to periodically mask out the one or more clock cycles of the clock in response to the control signal and generate the throttled clock.

15. (Previously Presented) The integrated circuit of claim 10, wherein,

one hundred percent of circuitry in the functional blocks can have the throttled clock stopped.

16. (Previously Presented) The integrated circuit of claim 10, wherein,

less than one hundred percent of circuitry in the functional blocks can have the throttled clock stopped.

17. (Currently Amended) The integrated circuit of claim 16, wherein,

only circuitry to which the throttled clock can be stopped is the throttled clock coupled and its frequency gradually throttled in response to the measure of the global functional activity meeting or exceeding the predetermined limit of activity.

18. (Currently Amended) The integrated circuit of claim 10, wherein,

the frequency of the throttled clock is gradually throttled OFF in response to the measure of the functional activity meeting or exceeding the predetermined limit of activity and

after being OFF for a predetermined period of time, the

throttled clock is then gradually throttled ON.

19. (Currently Amended) A clock generator comprising:

a free-running clock generator to generate a free-running clock;

an activity detector to receive a plurality of measures of local functional activity respectively associated with a plurality of [[each]] functional [[block]] blocks of an integrated circuit, to [[and]] generate a total measure of functional activity of the integrated circuit responsive to the plurality of measures of local functional activity, ~~the activity detector~~ to determine whether or not the total measure of functional activity ~~meets or~~ exceeds a predetermined limit of activity, and to generate an enable throttling signal responsive to a determination that the total measure of functional activity exceeds the predetermined limit of activity; and

a clock throttling controller coupled to the activity detector and the free-running clock generator, the clock throttling controller to generate a throttled clock to couple to the functional blocks of the integrated circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to circuitry of the functional blocks in response to the enable throttling signal.

20. (Previously Presented) A clock generator comprising:

a free-running clock generator to generate a free-running clock;

a thermal activity detector to generate a total measure of functional activity in an integrated circuit and to determine whether or not the total measure of functional activity meets or exceeds a thermal limit of activity to generate an enable thermal throttling signal; and

a clock throttling controller coupled to the thermal activity detector and the free-running clock generator, the clock throttling controller to generate a throttled clock to couple to functional blocks of the integrated circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to circuitry of the functional blocks in response to the enable thermal throttling signal,

wherein the clock throttling controller includes

a linear feedback shift register connected in a loop to generate a clock gating control signal, the clock gating control signal to selectively mask out clock cycles in the throttled clock to gradually reduce its frequency and to selectively insert clock cycles into the throttled clock to gradually increase its frequency, and

a state machine coupled to the linear feedback shift register to control the selective masking out of clock cycles and the selective inserting of clock cycles in the throttled clock to gradually throttle the frequency down to shut OFF the throttled clock and gradually throttle the frequency up from being shut OFF in response to the enable thermal throttling signal.

21. (Original) The clock generator of claim 20, wherein,

the clock throttling controller further includes,

a programmable counter to count a programmable delay time between changes in frequency of the throttled clock.

22. (Previously Presented) The method of claim 7, wherein,

the expected temperature level of the integrated circuit is one-hundred twenty five degrees centigrade, a maximum operating junction temperature for silicon.

23. (Previously Presented) The method of claim 7, wherein,

the expected temperature level of the integrated circuit is one-hundred ten degrees centigrade, a maximum case temperature under bias.

24. (Previously Presented) The method of claim 7, wherein,

the expected temperature level of the integrated circuit is eighty-five degrees centigrade, an operational case temperature.

25. (Previously Presented) The method of claim 7, wherein,

the expected temperature level of the integrated circuit is seventy degrees centigrade, a maximum ambient air temperature.

26. (Previously Presented) The method of claim 7, wherein,

the expected temperature level of the integrated circuit is fifty-five degrees centigrade, a maximum air temperature.

27. (Currently Amended) The integrated circuit of claim 10, wherein,

the ~~expected~~ predetermined limit of activity is proportional to a well known temperature level for integrated circuits.

28. (Previously Presented) The integrated circuit of

claim 27, wherein,

the well known temperature level for integrated circuits is one-hundred twenty five degrees centigrade, a maximum operating junction temperature for silicon.

29. (Previously Presented) The integrated circuit of claim 27, wherein,

the well known temperature level for integrated circuits is one-hundred ten degrees centigrade, a maximum case temperature under bias.

30. (Previously Presented) The integrated circuit of claim 27, wherein,

the well known temperature level for integrated circuits is eighty-five degrees centigrade, an operational case temperature.

31. (Previously Presented) The integrated circuit of claim 27, wherein,

the well known temperature level for integrated circuits is seventy degrees centigrade, a maximum ambient air temperature.

32. (Previously Presented) The integrated circuit of claim 27, wherein,

the well known temperature level for integrated

circuits is fifty-five degrees centigrade, a maximum air temperature.

33. (Currently Amended) The integrated circuit of claim 10, wherein,

the clock throttling controller gradually throttles down the frequency of the throttled clock to zero in response to the measure of the global functional activity meeting or exceeding the predetermined limit of activity.

34. (Previously Presented) The integrated circuit of claim 33, wherein,

after a predetermined period of time with the frequency of the throttled clock at zero, the clock throttling controller gradually throttles up the frequency of the throttled clock from zero.

35. (Previously Presented) The clock generator of claim 19, wherein,

the clock throttling controller gradually throttles down the frequency of the throttled clock to zero in response to the enable throttling signal.

36. (Previously Presented) The clock generator of claim 35, wherein,

after a predetermined period of time with the frequency

of the throttled clock at zero, the clock throttling controller gradually throttles up the frequency of the throttled clock from zero.

37. (Currently Amended) The clock generator of claim 19, wherein,

the predetermined limit of activity is proportional to a well known temperature level for integrated circuits.

38. (Previously Presented) The clock generator of claim 37, wherein,

the well known temperature level for integrated circuits is one-hundred ten degrees centigrade, a maximum case temperature under bias.

39. (Previously Presented) The clock generator of claim 37, wherein,

the well known temperature level for integrated circuits is eighty-five degrees centigrade, an operational case temperature.

40. (Previously Presented) The clock generator of claim 37, wherein,

the well known temperature level for integrated circuits is seventy degrees centigrade, a maximum ambient air temperature.

41. (Previously Presented) The clock generator of claim 37, wherein,

the well known temperature level for integrated circuits is fifty-five degrees centigrade, a maximum air temperature.

42. (New) The method of claim 1, wherein

a localized measure of activity in the integrated circuit is a number of logic gates within a functional block with an output change of state.

43. (New) The method of claim 1, wherein

a localized measure of activity in the integrated circuit is a number of nodes within a functional block switching from one logical state to another.

44. (New) The method of claim 1, wherein

the measure of global functional activity is generated by

weighting the plurality of localized measures of activity to generate weighted localized measures of activity, and

summing the weighted localized measures of activity together over a period of time.

45. (New) The integrated circuit of claim 10, wherein a localized measure of activity of a functional block in the integrated circuit is a number of logic gates within the functional block with an output change of state.

46. (New) The integrated circuit of claim 10, wherein a localized measure of activity of a functional block in the integrated circuit is a number of nodes within the functional block switching from one logical state to another.

47. (New) The integrated circuit of claim 10, wherein to generate the measure of global functional activity,

the activity detector to

weight the plurality of localized measures of activity to generate weighted localized measures of activity and

sum the weighted localized measures of activity together over a period of time.

48. (New) The integrated circuit of claim 13, wherein a localized measure of activity of a functional block in the integrated circuit is a number of logic gates within the functional block with an output change of state.

49. (New) The integrated circuit of claim 13, wherein a localized measure of activity of a functional block in the integrated circuit is a number of nodes within the functional block switching from one logical state to another.

50. (New) The integrated circuit of claim 13, wherein,

the activity detector receives measures of local functional activity associated with each functional block of the integrated circuit to measure the global functional activity of the integrated circuit.

51. (New) The integrated circuit of claim 13, wherein,

the activity detector receives measures of local functional activity associated with each functional block of the integrated circuit to determine the measure of the global functional activity of the integrated circuit,

the activity detector compares the measure of the global functional activity with the predetermined limit to determine if it is met or exceeded, and

the activity detector signals to the clock throttling controller whether or not the predetermined limit has been met or exceeded.

52. (New) The integrated circuit of claim 13, wherein,

the throttled clock is coupled to circuitry to which the throttled clock can be stopped, and

the frequency of the throttled clock is gradually throttled in response to the measure of the global functional activity meeting or exceeding the predetermined limit.

53. (New) The integrated circuit of claim 13, wherein,

the frequency of the throttled clock is gradually throttled OFF in response to the measure of the functional activity meeting or exceeding the predetermined limit and

after being OFF for a predetermined period of time, the throttled clock is then gradually throttled ON.

54. (New) The integrated circuit of claim 13, wherein

the measure of global functional activity of the integrated circuit is responsive to localized measures of activity,

the localized measures of activity corresponding respectively to local functional activity of a plurality of functional blocks in the integrated circuit.

55. (New) The integrated circuit of claim 54, wherein to generate the measure of global functional activity, the activity detector to weight the localized measures of activity to generate weighted localized measures of activity and sum the weighted localized measures of activity together over a period of time.

56. (New) The clock generator of claim 19, wherein, a measure of local functional activity of a functional block in the integrated circuit is a number of logic gates within the functional block with an output change of state.

57. (New) The clock generator of claim 19, wherein a measure of local functional activity of a functional block in the integrated circuit is a number of nodes within the functional block switching from one logical state to another.

58. (New) The clock generator of claim 19, wherein, to generate the total measure of functional activity, the activity detector to weight the measures of local functional activity to generate weighted measures of local functional activity and sum the weighted measures of local functional activity

together over a period of time.

59. (New) The clock generator of claim 20, wherein, the total measure of functional activity is responsive to a plurality of measures of local functional activity of functional blocks in the integrated circuit.

60. (New) The clock generator of claim 59, wherein a measure of local functional activity of a functional block in the integrated circuit is a number of nodes within the functional block switching from one logical state to another, a number of logic gates within the functional block with an output change of state, or a combination thereof.